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10/536,460	05/25/2005	Seiji Miura	XA-10365	6477

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
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EXAMINER	
GU, SHAWN X	
ART UNIT	**PAPER NUMBER**
2189	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,460	MIURA ET AL.	
	Examiner	Art Unit	
	Shawn X. Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-18,21,24,25,27 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-18,21,24,25,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/6/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 6 December 2005 was filed on or after the mailing date of the application on 25 May 2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the Examiner.

Double Patenting

3. Claim 4 of U.S. Patent 6,587.393, claims 17-19 of U.S. Patent 6,392,950 and claims 2-13 of U.S. Patent 6,411,561 contain every element of claim 1 of the instant application and as such anticipate claim 1 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-

type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 18 states the non-volatile memory performs the tasks of error detection, error correction and address replacement. The Examiner is unable to understand how a storage device such as a non-volatile memory is able to perform or execute the above tasks. It would be more appropriate to claim that the non-volatile memory supports the performing or execution of the above tasks. Appropriate correction is required.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 10 and 12-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites "the similar memory size" on line 4. The limitation lacks antecedent basis and the term "similar memory size" is vague and indefinite. The Applicant should provide a specific range of values that are considered to be similar. Appropriate correction is required.

Claims 12-14 recite "the data-hold operation of the dynamic random access memory". This limitation lacks antecedent basis and renders the claims vague and indefinite. The Examiner is unable to form an adequate understanding of the claims and the claims are rejected under 35 U.S.C 102 (b) as follows with the broadest reasonable interpretation. Appropriate correction is required.

Claim 13 is dependent on the cancelled claim 11 and should be either cancelled or dependent on a pending claim. The Examiner is unable to evaluate the claim's merits as the exact metes and bounds of the claim are unclear and the claim as a result is vague and indefinite. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-9, 12, 18, 21, 24, 25, 27 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiraki et al. [US 6,324,103 B2] (hereinafter "Hiraki").

Per claim 1, Hiraki teaches a memory module including a non-volatile memory, a dynamic random access memory, a static random access memory and a control circuit that accesses the non-volatile memory, the dynamic random access memory and the static random access memory (see Figs 1, 14, 17 and 20), comprising: a dynamic random access memory interface for accessing the dynamic random access memory from a device outside the memory module; and a static random access memory interface for accessing the static random access memory (data terminals, col. 6, lines 49-67).

Per claim 2, Hiraki further teaches immediately after power is turned on (col. 13, lines 18-29 and Fig 3), data in a predetermined address region (col. 20, lines 41-45 and Fig.15) of the non-volatile memory is transferred to the static random access memory.

Per claim 3, Hiraki further teaches immediately after power is turned on (col. 13, line 18-29 and Fig 3), data in a predetermined address region (col. 20, lines 41-45 and Fig.15) of the non-volatile memory is transferred to the dynamic random access memory.

Per claim 4, Hiraki further teaches data transfer between the non-volatile memory and the dynamic random access memory is performed according to an instruction via the dynamic random access memory interface ("Executing reading and setting operations", see col. 4, lines 1-10, col. 20, lines 57-67 and col.21, lines 1-3).

Per claim 5, Hiraki further teaches data transfer between the non-volatile memory and the static random access memory is performed according to an instruction via the static random access memory interface ("Executing reading and setting operations", see col. 4, lines 1-10, col. 20, lines 57-67 and col.21, lines 1-3).

Per claim 6, Hiraki further teaches in data transfer from the non-volatile memory to the static random access memory or the dynamic random access memory, data acquired by correcting an error is transferred ("repair information", see col. 3, lines 25-67 and col. 4, lines 1-10).

Per claim 7, Hiraki further teaches in data transfer from the static random access memory or the dynamic random access memory to the non-volatile memory, an

address replacement process is executed ("repair address register", see Fig. 1, 14 and 17; "repairable redundancy construction" and "reprogramming the flash memory", see col. 12, lines 59-67, col. 13, lines 1-17, col. 14, 8-67 and col. 15, lines 1-22).

Per claim 8, Hiraki further teaches a boot program is held in the non-volatile memory (col. 3, lines 42-49, col. 6, lines 30-35 and 55-67, and col. 10, lines 25-35).

Per claim 9, Hiraki further teaches data transfer range data showing a range of data transferred from the non-volatile memory to the dynamic random access memory at initial time when operating power is turned on is held in the non-volatile memory (col. 14, lines 26-67 and col. 15, lines 1-22).

Per claim 12, Hiraki further teaches the data-hold operation of the dynamic random access memory is executed inside the memory module (see the reference cirted in the rejections of claims 6, 8 and 9).

Per claim 18, Hiraki further teaches the non-volatile memory performs error detection, error correction and address replacement (see the reference cited in the rejections of claims 2-8).

Per claim 21, Hiraki further teaches the dynamic random access memory is equipped with plural interfaces (see Fig. 1, 14, 17 and 20).

Per claim 24, Hiraki further teaches the dynamic random access memory is equipped with a control circuit for processing access from the device outside the memory module and a control circuit for independently accessing the non-volatile memory (see Fig. 1, 14, 17 and 20 and "reprogramming the flash memory", see col. 14, lines 8-67 and col. 15, lines 1-22).

Per claim 25, Hiraki further teaches the dynamic random access memory is equipped with a control circuit for independently accessing the non-volatile memory and a circuit for subordinately processing the access (see Fig. 1, 14, 17 and 20).

Per claim 27, Hiraki further teaches the non-volatile memory is equipped with a static random access memory, an error detecting and correcting circuit and an address replacement circuit (see Fig 1, 14, 17 and 20; the term "equipped" is broadly interpreted as "supplemented", "attached", and/or "enhanced").

Per claim 28, Hiraki further teaches the non-volatile memory is equipped with plural interfaces (see Fig. 1, 14, 17 and 20).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 10, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraki [US 6,324,103 B2].

Per claim 10, Hiraki further teaches the non-volatile memory and the dynamic random access memory have the similar memory size (see col. 10, lines 44-60 and col. 11, lines 33-40; both memories stores data and programs, hence their memory sizes are similar), but fails to teach the static random access memory (SRAM) has memory size equal to/smaller than 1/1000 of that of the non-volatile memory. However, Hiraki teaches that the SRAM is utilized as a quick access register file (see col. 11, lines 8-10), which implies small memory size for the SRAM. Hiraki further teaches the flash memory stores boot programs, repair information and other data, implying the flash memory's memory size fairly large compared to that of the SRAM, although Hiraki does not teach the flash is 1000 or greater times the size of the SRAM. The specific ratio between the sizes of the two memories would be dependent on the design specification of the article in Hiraki's invention. Therefore, it is clear that Hiraki already teaches the flash memory size is much greater than that of the SRAM, and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that making the flash memory 1000 or greater times the size of the SRAM is design specification dependent.

Per claim 14, Hiraki does not disclose access from the device outside the memory module is first preceded; the data-hold operation of the dynamic random access memory inside the memory module is second preceded; and data transfer between the non-volatile memory and the static random access memory or the dynamic random access memory is third preceded. However, the order of the execution of these operations are dependent on the issue timing and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that if the access from the device outside the memory module is issued first, the data-hold operation is issued second with a large timing delay, and the data transfer is issued third with another large timing delay, then the order of execution of these operations would be identical to the order described by the claim.

Per claim 15, Hiraki further teaches access to the non-volatile memory and the dynamic random access memory from the device outside the memory module is made via an interface of the DRAM (see Figs 1, 14, 17 and 20), but fails to teach the DRAM is a synchronous DRAM (SDRAM). However, it is clear to that SDRAMs can run at a higher clock speed than conventional DRAMs and therefore provides lower access latency than convention DRAMs and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use a SDRAM in Hiraki's invention instead of a convention DRAM to reduce access latency.

12. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraki [US 6,324,103 B2] and Tanzawa et al. [6,072,719] (hereinafter "Tanzawa").

Per claims 16 and 17, Hiraki already substantially discloses the claims as set forth above in claim 15 and further teaches the non-volatile memory is a flash memory (see Fig 1, 14, 17 and 20). Hiraki does not teach the flash memory is a NAND flash memory or a AND flash memory. However, Tanzawa teaches the use of both NAND and AND flash memories, which are suited to flash devices requiring high capacity data storage. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use either a NAND flash memory or an AND flash memory in Hiraki's invention to provide large data storage capacity.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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19 May 2007